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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/014,287	11/09/2001	Ronald Pasqualini	072219-0261705 (P05090)	2344

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EXAMINER	
MAI, TAN V	

ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 08/31/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/014,287	PASQUALINI, RONALD	
	Examiner	Art Unit	
	Tan V Mai	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/22, 7/29, 8/5, 9/13 & 11/13/02*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 August 2002* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The abstract of the disclosure is objected to because the Abstract contains the undefined acronym "CMOS". All such acronyms should be defined at the instance of their first use within the Abstract. Correction is required. See MPEP § 608.01(b).

2. Claims 17-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 17, the claim recites "further comprising: a second adder cell..."; however, the essential interconnection between the first and second is missing. Similarly noted claims 18 & 21-22.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (c) he has abandoned the invention.
>
> (d) the invention was first patented or caused to be patented, or was the subject of an inventor's certificate, by the applicant or his legal representatives or assigns in a foreign country prior to the date of the application for patent in this country on an application for patent or inventor's certificate filed more than twelve months before the filing of the application in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

(f) he did not himself invent the subject matter sought to be patented.

(g)(1) during the course of an interference conducted under section 135 or section 291, another inventor involved therein establishes, to the extent permitted in section 104, that before such person's invention thereof the invention was made by such other inventor and not abandoned, suppressed, or concealed, or (2) before such person's invention thereof, the invention was made in this country by another inventor who had not abandoned, suppressed, or concealed it. In determining priority of invention under this subsection, there shall be considered not only the respective dates of conception and reduction to practice of the invention, but also the reasonable diligence of one who was first to conceive and last to reduce to practice, from a time prior to conception by the other.

4. Claims 1-2, 4, 6-16 and 23-24 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Takahashi.

As per independent claim 1, Takahashi teaches, e.g., see Figs. 1A, 2A & 5-7, the claimed combination. For example, the "first adder cell" comprises:

a first logic gate (element 12 of Fig. 1A, element 22 of Fig. 2A, element 30 of Fig. 5, elements 40 &42 of Fig. 6 or element 50 of Fig. 7);

a first inverter circuit (elements INV103 & INV102 of Fig. 1A, elements INV202 & INV203 of Fig. 2A, element INV303 & XNOR gate 32 of Fig. 5, elements INV406, INV405 & INV402 of Fig. 6 or elements INV303 & INV501 of Fig. 7);

a first carry out circuit [which provides Cout in Figs. 5-7]; and

a first sum circuit [which provides Sout in Figs. 5-7].

As per dependent claim 2, Takahashi teaches the claimed feature.

As per dependent claim 4, Takahashi teaches the claimed feature.

As per dependent claim 6, Takahashi teaches the claimed feature.

As per dependent claim 7, Takahashi teaches the claimed feature.

As per dependent claim 8, Takahashi teaches the claimed feature.

As per dependent claim 9, Takahashi teaches the claimed feature.

As per dependent claim 10, Takahashi teaches the claimed feature.

As per dependent claim 11, Takahashi teaches the claimed feature.

As per dependent claim 12, Takahashi teaches the claimed feature.

As per dependent claim 13, Takahashi teaches the claimed feature.

As per dependent claim 14, Takahashi teaches the claimed feature.

As per dependent claim 15, Takahashi teaches the claimed feature.

As per dependent claim 16, the claim details the first logic gate. Takahashi teaches all the claimed features.

As per dependent claim 23, Takahashi teaches the claimed feature.

As per dependent claim 24, Takahashi teaches the claimed feature, i.e., when the full adder is operated as a subtractor.

5. Claims 1-3, 5-12, 14-17 and 23-24 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Hmida et al.

As per independent claim 1, Hmida et al teach, e.g., see Figs. 2-5, the claimed combination. For example, the "first adder cell" comprises:

a first logic gate (element 100 of Fig. 2, element 109 of Fig. 3, element 130 of Fig. 4, element 140 or 150 of Fig. 5);

a first inverter circuit (inverter in element 200 & inverter 400 of Fig. 2, inverter in element 250 & inverter 450 of Fig. 3, inverter in element 260 & inverter 460 of Fig. 4, inverter 700 & inverter 470 of Fig. 5)

a first carry out circuit [which provides RiS, Ri+1S or inverted RiS in Figs. 2-5]; and

a first sum circuit [which provides Si or Si+1 in Figs. 2-5].

As per dependent claim 2, Hmida et al teach the claimed feature.

As per dependent claim 3, Hmida et al teach the claimed feature.

As per dependent claim 5, Hmida et al teach the claimed feature.

As per dependent claim 6, Hmida et al teach the claimed feature, e.g., see Fig. 5, inverter 700 coupled to the first carry out circuit 370.

As per dependent claim 7, Hmida et al teach the claimed feature.

As per dependent claim 8, Hmida et al teach the claimed feature.

As per dependent claim 9, Hmida et al teach the claimed feature.

As per dependent claim 10, Hmida et al teach the claimed feature.

As per dependent claim 11, Hmida et al teach the claimed feature.

As per dependent claim 12, Hmida et al teach the claimed feature.

As per dependent claim 14, Hmida et al teach the claimed feature, e.g., see Fig. 4.

As per dependent claim 15, Hmida et al teach the claimed feature.

As per dependent claim 16, the claim details the first logic gate. Hmida et al teach all the claimed features.

As per dependent claim 17, the claim adds a second adder cell. Hmida et al teach all the claimed features, e.g., see Fig. 5.

As per dependent claim 23, Hmida et al teach the claimed feature.

As per dependent claim 24, Hmida et al teach the claimed feature, i.e., when the full adder is operated as a subtractor.

6. Claims 1-6, 8-13, 15, 17-19 and 23-24 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Mazin et al.

As per independent claim 1, Mazin et al teach, e.g., see Figs. 1-3, the claimed combination. For example, the "first adder cell" comprises:

a first logic gate (exclusive OR gate of Figs. 1 &3);

a first inverter circuit (inverters 17/19 & 15 of Fig. 1, inverter 27/29 & 25 of Fig. 3);

a first carry out circuit [which provides inverted Cout or Cout]; and

a first sum circuit [which provides SUM or inverted SUM].

As per dependent claim 2, Mazin et al teach the claimed feature.

As per dependent claim 3, Mazin et al teach the claimed feature, e.g., see Fig. 1, first input signal A.

As per dependent claim 4, Mazin et al teach the claimed feature, e.g., see Fig. 2, first inverted signal A.

As per dependent claim 5, Mazin et al teach the claimed feature, e.g., see Fig. 2.

As per dependent claim 6, Mazin et al teach the claimed feature, e.g., see Fig. 1.

As per dependent claim 8, Mazin et al teach the claimed feature.

As per dependent claim 9, Mazin et al teach the claimed feature.

As per dependent claim 10, Mazin et al teach the claimed feature.

As per dependent claim 11, Mazin et al teach the claimed feature.

As per dependent claim 12, Mazin et al teach the claimed feature.

As per dependent claim 13, Mazin et al teach the claimed feature.

As per dependent claim 15, Mazin et al teach the claimed feature.

As per dependent claim 17, the claim adds a second adder cell. Mazin et al teach the claimed features, e.g., see Fig. 3.

As per dependent claim 18, the claim adds a third adder cell. Mazin et al teach the claimed features, e.g., see Fig. 3.

As per dependent claim 19, the claim adds the "row" feature. Mazin et al teach the claimed features, e.g., see Fig. 3 shows an array full adder cells.

As per dependent claim 23, Mazin et al teach the claimed feature.

As per dependent claim 24, Mazin et al teach the claimed feature, i.e., when the full adder is operated as a subtractor.

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 14 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mazin et al.

Mazin et al have been discussed in paragraph #6 above.

As per dependent claim 14, the claim adds a first buffer inverter. The feature is old and well known in the art, e.g., see Hmida et al (Fig. 4, inverter 600) or Takahashi (Figs. 5-7, inverters coupled to the Cout). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to design the claimed invention according to Mazin et al's teachings because the device is a full adder cell as claimed.

As per dependent claim 20, the claim adds the "row" features. Mazin et al do show different full adder cells in two rows. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to design the claimed invention according to Mazin et al's teachings because the reference shows array of full adder cells having different full adder cells.

As per dependent claim 21, the claim adds a second adder cell. Mazin et al teach the claimed features, e.g., see Fig. 3.

As per dependent claim 22, the claim adds a third adder cell. Mazin et al teach the claimed features, e.g., see Fig. 3.

9. Claims 3, 5 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi in view of either Hmida et al or Mazin et al.

Takahashi, Hmida et al and Mazin et al have discussed in paragraphs above.

As per dependent claim 3, the claim adds "wherein the first received signal is the first input signal". The feature is old and well known in the art, e.g., see Hmida et al

(Figs. 2-5, signal Ai) or Mazin et al (Fig. 1, signal A). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine either Hmida et al or Mazin et al's feature in Takahashi, thereby making the claimed invention, because the proposed device is a full adder having all the features as claimed.

As per dependent claim 5, the claim adds "wherein the second received signal is the third input signal". The feature is old and well known in the art, e.g., see Hmida et al (Figs. 2-3, signal Ri-S; Fig. 4, output of inverter 500; Fig. 5, output of inverter 800) or Mazin et al (Fig. 2, output of inverter 29). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine either Hmida et al or Mazin et al's feature in Takahashi, thereby making the claimed invention, because the proposed device is a full adder having all the features as claimed.

As per dependent claim 17, the claim adds a second adder cell. Hmida et al and Mazin et al do show the claimed feature. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine either Hmida et al or Mazin et al's feature in Takahashi, thereby making the claimed invention, because the proposed device is an adder circuit having all the features as claimed.

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Cited references are art of interest.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan V. Mai whose telephone number is (703) 305-9761. The examiner can normally be reached on Tue-Fri from 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki, can be reached on (703) 305-9662. The fax phone numbers for the organization where this application or proceeding is assigned are:

Official (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

TAN V. MAI
PRIMARY EXAMINER